FIG. 1

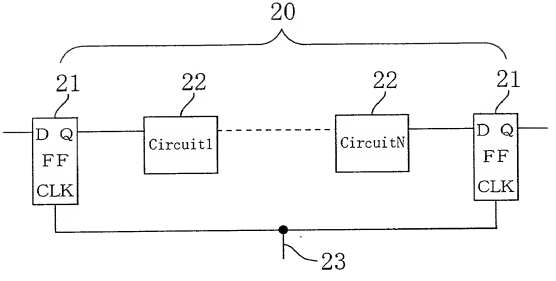


FIG. 2

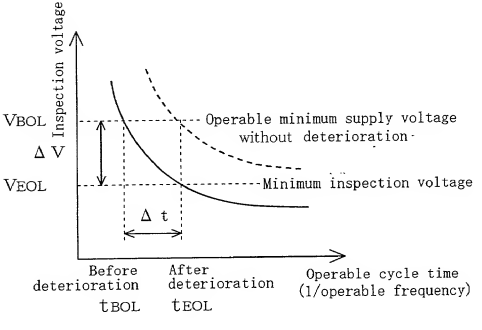


FIG. 3

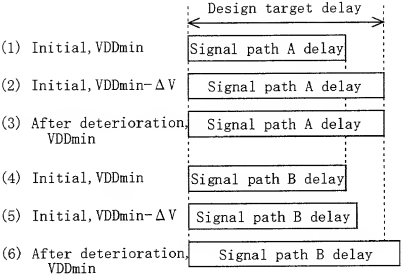


FIG. 4

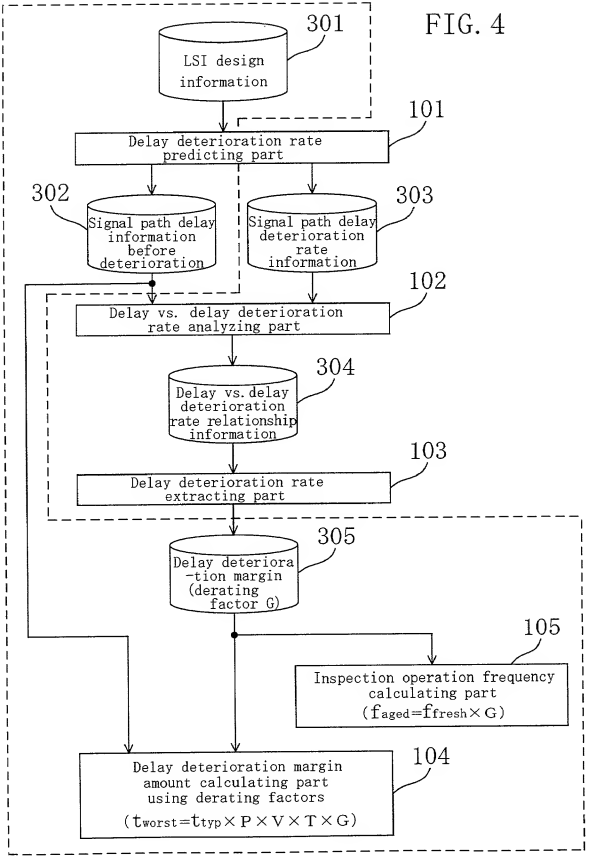

301
LSI design information
101
Delay deterioration rate predicting part
302
Signal path delay information before deterioration
303
Signal path delay deterioration rate information
102
Delay vs. delay deterioration rate analyzing part
304
Delay vs. delay deterioration rate relationship information
103
Delay deterioration rate extracting part
305
Delay deteriora -tion margin (derating factor G)
105
Inspection operation frequency calculating part
($f_{aged}=f_{fresh}\times G$)
104
Delay deterioration margin amount calculating part using derating factors
($t_{worst}=t_{typ}\times P\times V\times T\times G$)

FIG. 5

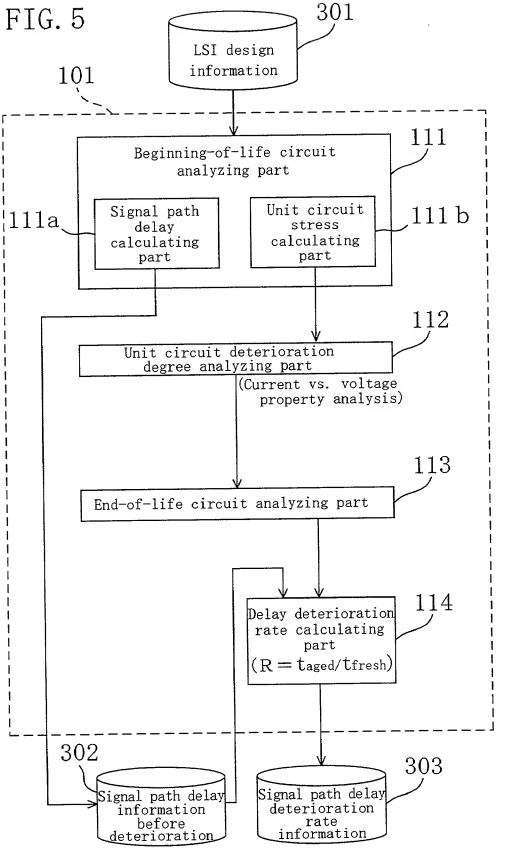

301
LSI design information
101
111
Beginning-of-life circuit analyzing part
111a
Signal path delay calculating part
Unit circuit stress calculating part
111 b
112
Unit circuit deterioration degree analyzing part
(Current vs. voltage property analysis)
113
End-of-life circuit analyzing part
114
Delay deterioration rate calculating part
(R = taged/tfresh)
302
Signal path delay information before deterioration
303
Signal path delay deterioration rate information

FIG. 6

Signal path	Signal path delay before deterioration t_{fresh} (ns) (Signal path delay information before deterioration 302)	Signal path delay after deterioration t_{aged} (ns)	Signal path delay deterioration rate $R = t_{aged}/t_{fresh}$ (Signal path delay deterioration rate information 303)
Path 1	3.0	3.036	1.012
Path 2	4.7	4.771	1.015
⋮	⋮	⋮	⋮
Path M	0.3	3.090	1.030

FIG. 7

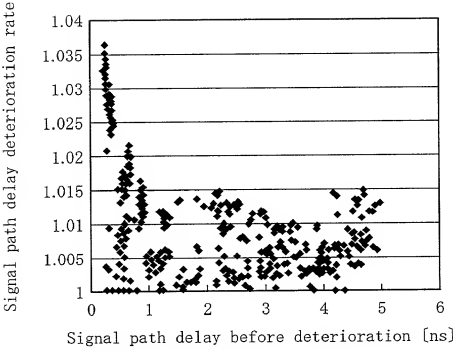

Signal path delay deterioration rate
1.04
1.035
1.03
1.025
1.02
1.015
1.01
1.005
1
0
1
2
3
4
5
6
Signal path delay before deterioration [ns]

FIG. 8

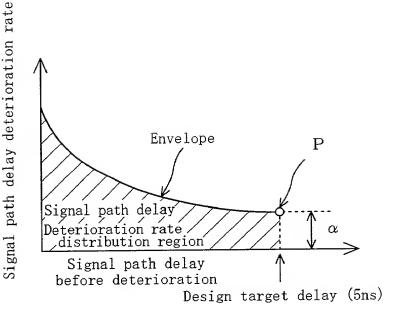

Signal path delay deterioration rate
Envelope
P
Signal path delay
Deterioration rate
distribution region
α
Signal path delay
before deterioration
Design target delay (5ns)

FIG. 9

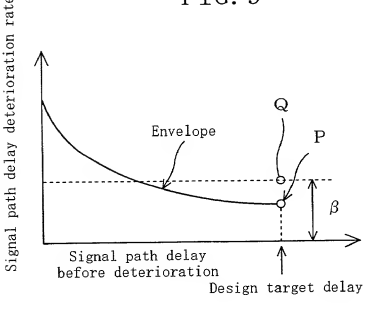

Signal path delay deterioration rate
Q
Envelope
P
β
Signal path delay
before deterioration
Design target delay

FIG. 10

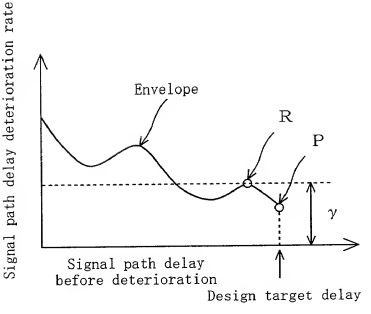

Signal path delay deterioration rate
Envelope
R
P
γ
Signal path delay
before deterioration
Design target delay

FIG. 11

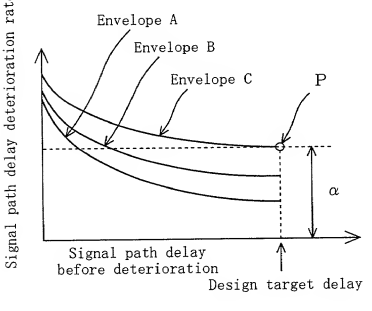

Signal path delay deterioration rate
Envelope A
Envelope B
Envelope C
P
α
Signal path delay
before deterioration
Design target delay

FIG. 12

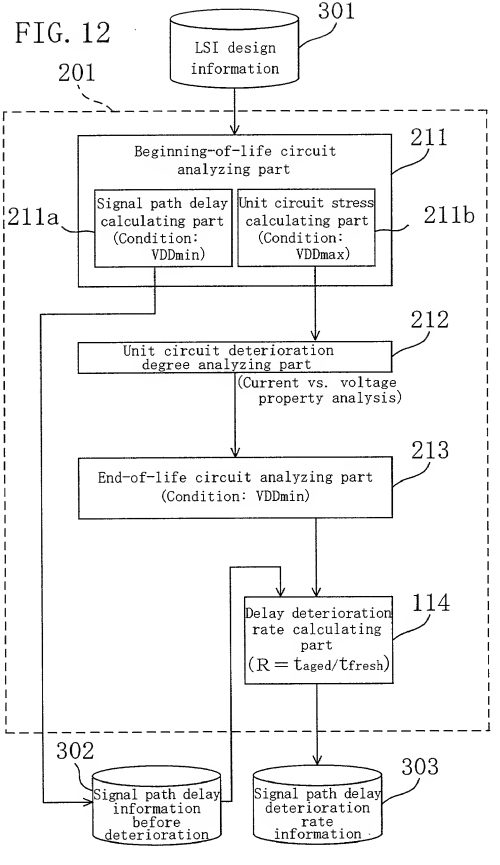

301
LSI design information
201
211
Beginning-of-life circuit analyzing part
211a
Signal path delay calculating part (Condition: VDDmin)
Unit circuit stress calculating part (Condition: VDDmax)
211b
212
Unit circuit deterioration degree analyzing part
(Current vs. voltage property analysis)
213
End-of-life circuit analyzing part (Condition: VDDmin)
114
Delay deterioration rate calculating part
(R = τaged/τfresh)
302
Signal path delay information before deterioration
303
Signal path delay deterioration rate information

FIG. 13

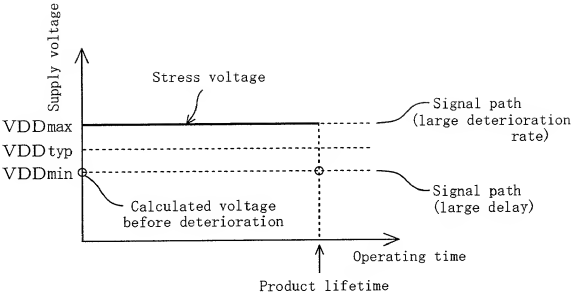

Supply voltage
Stress voltage
VDDmax
VDDtyp
VDDmin
Signal path
(large deterioration
rate)
Signal path
(large delay)
Calculated voltage
before deterioration
Operating time
Product lifetime

FIG. 14

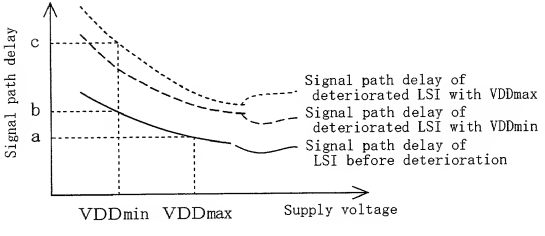
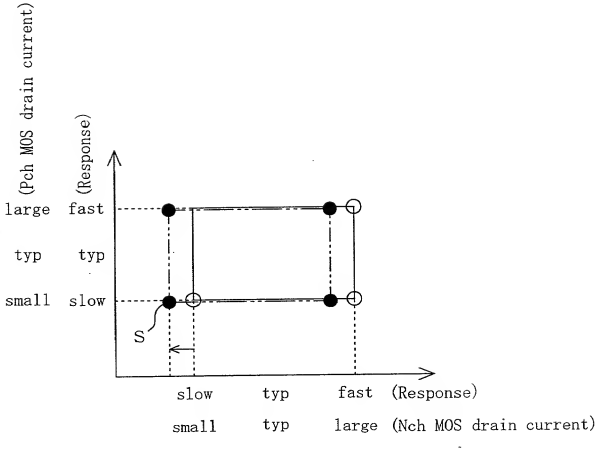

Signal path delay
c
b
a
Signal path delay of
deteriorated LSI with VDDmax
Signal path delay of
deteriorated LSI with VDDmin
Signal path delay of
LSI before deterioration
VDDmin VDDmax
Supply voltage

FIG. 15


(Pch MOS drain current)
(Response)
large
fast
typ
typ
small
slow
S
slow
typ
fast
(Response)
small
typ
large
(Nch MOS drain current)